Notice of Allowability	Application No.	Applicant(s)	
	09/724,585	BEARDSLEE ET AL.	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *22 July 2004*.

2. ☒ The allowed claim(s) is/are *1-6 and 8-47*.

3. ☒ The drawings filed on *28 November 2000* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER

DETAILED ACTION

Introduction

1. This communication is in response to the Applicants' amendments dated July 22, 2004. Claims 1, 4, 8-10, 13, 14, 16, 21 and 23 were amended. Claim 7 was deleted. Claims 25-47 were added. Claims 1-6 and 8-47 of the application are pending.

Examiner's Amendment

2. Authorization for this examiner's amendment was given in a telephone interview with Mr. Richard Thill, assistant to Mr. Robert B. O'Rourke on November 4, 2004.

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

3. The application has been amended as follows:

In Claim 1, Line 8, change:

"determining configuration information based on the certain activated design visibility, design patching or design control aspects"

to

-- determining configuration information of said instrumentation circuitry based on the certain activated design visibility, design patching or design control aspects --.

In Claim 21, Line 9, change:

"determining configuration information based on the certain activated aspects"

to

-- determining configuration information of said instrumentation circuitry based on the certain activated aspects --.

In Claim 25, Line 8, change:

"determining configuration information based on the certain activated design visibility, design patching or design control aspects"

to

-- determining configuration information of said instrumentation circuitry based on the certain activated design visibility, design patching or design control aspects --.

In Claim 44, Line 9, change:

"determining configuration information based on the certain activated aspects"

to

-- determining configuration information of said instrumentation circuitry based on the certain activated aspects --.

Reasons for Allowance

4. Claims 1-6 and 8-47 of the application are allowed over prior art of record.

5. The following is an Examiner's statement of reasons for the indication of allowable subject matter:

The closest prior art of record shows:

(1) analyzing and debugging digital circuits constructed from HDL source using logic synthesis; a method for displaying results of synthesized circuit analysis visually near the HDL source specification; the synthesis process translates the HDL source code into an initial circuit; a more efficient circuit is constructed from initial circuit by logic optimization; circuit analysis results corresponding to the points in the final circuit that can be traced to the initial circuit, can be directly related to the appropriate part of the HDL source; provides a method of introducing

additional points in the design that remain traceable through the optimization process; (**Gregory et al.,** U. S. Patent 5,937,190);

(2) a method and system that improve the model build and simulation processes to allow a designer to easily instrument and monitor a simulation model; instrumentation modules written in the hardware description language are used to monitor the operation of digital circuit designs; utilizes the inherent hierarchical and modular nature of the HDL to provide simulation instrumentation in the form of HDL entities for digital circuit design simulation models; allows to accurately monitor the characteristics of specific sub-modules of large scale design to efficiently and accurately diagnose the problems and assess the correctness of the overall design; (**Bargh et al.,** U. S. Patent 6,195,629);

(3) debugging synthesizable code at the register transfer level during gate-level simulation; methods of instrumenting synthesizable RTL source code to enable debugging support akin to high level language programming environment; includes instrumentation logic indicative of the execution status of at least one synthesizable statement; evaluation of the instrumentation logic during simulation of the gate-level netlist enables RTL debugging; gate-level netlist is modified to provide instrumentation signals corresponding to synthesizable statements within RTL source code; (**Burgun et al.**, U. S. Patent 6,336,087); and

(4) DFT tools to embed test circuitry into the design of the digital circuits; the design methodology for the IC includes initially designing the circuit using a software design tool; simulating the overall functionality of the IC or the individual circuits; generating the embedded test circuitry to test the individual circuits; generating the test vectors for functionally testing the device by an ATE; (**Eldridge et al.**, U. S. Patent 6,551,844)

5.1 Applicant's first set of claims consists of Claims 1-6 and 8-20.

Independent Claim 1 is directed to a method for debugging a fabricated integrated circuit product having instrumentation circuitry included therein. The claim identifies the uniquely distinct features of:

"as part of the integrated circuit product's design process generating the instrumentation circuitry at least by activating certain aspects of the instrumentation circuitry for examining and/or modifying the integrated circuit product", "after the integrated circuit product has been fabricated configuring the instrumentation circuitry in accordance with the configuration information" and "receiving debug data from the configured instrumentation circuitry operating within the integrated circuit product; translating the debug data into HDL-related debug information; and relating the HDL-related debug information to the HDL description".

The closest prior art fails to teach or fairly suggest as part of the integrated circuit product's design process generating the instrumentation circuitry at least by activating certain aspects of the instrumentation circuitry for examining and/or modifying the integrated circuit product; after the integrated circuit product has been fabricated configuring the instrumentation circuitry in accordance with the configuration information; and receiving debug data from the configured instrumentation circuitry operating within the integrated circuit product; translating the debug data into HDL-related debug information; and relating the HDL-related debug information to the HDL description. Therefore, Claims 1-6 and 8-20 are deemed novel and allowable.

5.2 Applicant's second set of claims consists of Claims 21-24.

Independent Claim 21 is directed to a method for debugging a fabricated integrated circuit product having instrumentation circuitry included therein. The claim identifies the uniquely distinct features of:

"as part of the integrated circuit product's design process generating the instrumentation circuitry at least by activating certain aspects of the instrumentation circuitry for examining and/or modifying the integrated circuit product", "after the integrated circuit product has been fabricated configuring the instrumentation circuitry in accordance with the configuration information" and "receiving debug data from the configured instrumentation circuitry operating within the integrated circuit product; translating the debug data into HDL-related debug information; relating the HDL-related debug information to the high-level HDL description; and thereafter retrieving circuit status information for the integrated circuit product via the instrumentation circuitry".

The closest prior art fails to teach or fairly suggest as part of the integrated circuit product's design process generating the instrumentation circuitry at least by activating certain aspects of the instrumentation circuitry for examining and/or modifying the integrated circuit product; after the integrated circuit product has been fabricated configuring the instrumentation circuitry in accordance with the configuration information; and receiving debug data from the configured instrumentation circuitry operating within the integrated circuit product; translating the debug data into HDL-related debug information; relating the HDL-related debug information

to the high-level HDL description; and thereafter retrieving circuit status information for the integrated circuit product via the instrumentation circuitry. Therefore, Claims 21-24 are deemed novel and allowable.

5.3 Applicant's third set of claims consists of Claims 25-43.

Independent Claim 25 is directed to an article of manufacture including program code which, when executed by a machine, causes the machine to perform method for debugging a fabricated electronic system having instrumentation circuitry included therein. The claim identifies the uniquely distinct features of:

"as part of the integrated circuit product's design process generating the instrumentation circuitry at least by activating certain aspects of the instrumentation circuitry for examining and/or modifying the integrated circuit product", "after the integrated circuit product has been fabricated configuring the instrumentation circuitry in accordance with the configuration information" and "receiving debug data from the configured instrumentation circuitry operating within the integrated circuit product; translating the debug data into HDL-related debug information; and relating the HDL-related debug information to the HDL description".

The closest prior art fails to teach or fairly suggest as part of the integrated circuit product's design process generating the instrumentation circuitry at least by activating certain aspects of the instrumentation circuitry for examining and/or modifying the integrated circuit product; after the integrated circuit product has been fabricated configuring the instrumentation circuitry in accordance with the configuration information; and receiving debug data from the

configured instrumentation circuitry operating within the integrated circuit product; translating the debug data into HDL-related debug information; and relating the HDL-related debug information to the HDL description. Therefore, Claims 25-43 are deemed novel and allowable.

5.4 Applicant's fourth set of claims consists of Claims 44-47.

Independent Claim 44 is directed to an article of manufacture including program code which, when executed by a machine, causes the machine to perform a method for debugging a fabricated integrated circuit product having instrumentation circuitry included therein. The claim identifies the uniquely distinct features of:

"as part of the integrated circuit product's design process generating the instrumentation circuitry at least by activating certain aspects of the instrumentation circuitry for examining and/or modifying the integrated circuit product", "after the integrated circuit product has been fabricated configuring the instrumentation circuitry in accordance with the configuration information" and "receiving debug data from the configured instrumentation circuitry operating within the integrated circuit product; translating the debug data into HDL-related debug information; relating the HDL-related debug information to the high-level HDL description; and thereafter retrieving circuit status information for the integrated circuit product via the instrumentation circuitry".

The closest prior art fails to teach or fairly suggest as part of the integrated circuit product's design process generating the instrumentation circuitry at least by activating certain aspects of the instrumentation circuitry for examining and/or modifying the integrated circuit

product; after the integrated circuit product has been fabricated configuring the instrumentation circuitry in accordance with the configuration information; and receiving debug data from the configured instrumentation circuitry operating within the integrated circuit product; translating the debug data into HDL-related debug information; relating the HDL-related debug information to the high-level HDL description; and thereafter retrieving circuit status information for the integrated circuit product via the instrumentation circuitry. Therefore, Claims 44-47 are deemed novel and allowable.

6. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 571-272-3717. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska, can be reached on 571-272-3716. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

K. Thangavelu
Art Unit 2123
November 4, 2004

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER